Central™
Semiconductor Corp.

PROCESS CP230

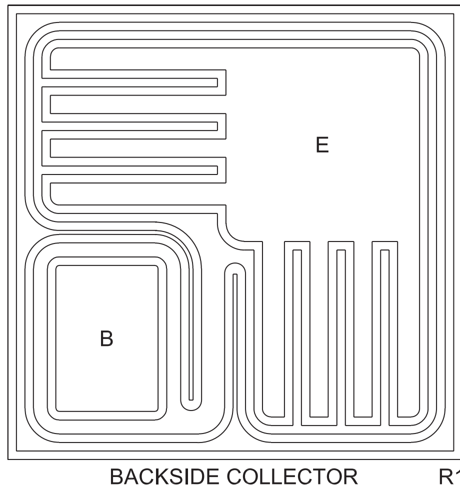
Power Transistor

NPN - Silicon Darlington Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL BASE
Die Size	80 X 80 MILS
Die Thickness	8 MILS
Base Bonding Pad Area	18 X 27 MILS
Emitter Bonding Pad Area	34 X 34 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ti/Pd/Ag (20,000Å)

Geometry



BACKSIDE COLLECTOR R1

GROSS DIE PER 4 INCH WAFER

1,445

PRINCIPAL DEVICE TYPES

CZT122
CJD122

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

R1 (22-August 2008)

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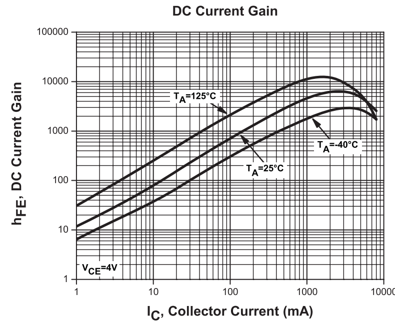
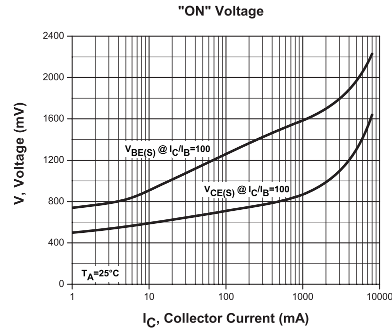
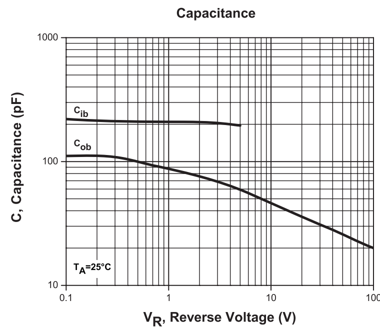
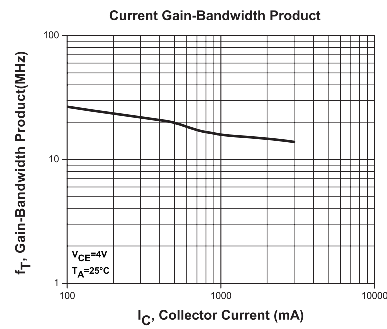
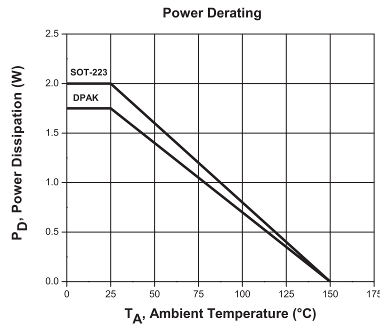
Typical Electrical Characteristics











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